WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device having a control gate electrode and a floating gate electrode provided on a semiconductor substrate to have their respective side surfaces in opposed relation, the device comprising:

a gate insulating film formed on the semiconductor substrate;

the control gate electrode formed on the gate insulating film;

a protective insulating film deposited on each of the side surfaces of the control gate electrode to protect the control gate electrode during formation of the floating gate electrode;

the floating gate electrode opposed to one of the side surfaces of the control gate electrode with the protective insulating film interposed therebetween so as to be capacitively coupled to the control gate electrode;

a tunnel insulating film formed between the floating gate electrode and the semiconductor substrate;

a drain region formed in a region of the semiconductor substrate containing a portion underlying the floating gate electrode; and

a source region formed in a region of the semiconductor substrate opposite to the drain region relative to the control gate electrode.

2. The device of claim 1, wherein the protective insulating film has a uniform thickness.

3. The device of claim 1, wherein the gate insulating film has a uniform thickness.

4. The device of claim 1, wherein the tunnel insulating film has a uniform thickness.

5. The device of claim 1, further comprising an insulating film formed between the control gate electrode and the protective insulating film.

6. The device of claim 1, wherein the protective insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

7. The device of claim 1, wherein the semiconductor substrate has a stepped portion formed to be covered up with the floating gate electrode.

8. A nonvolatile semiconductor memory device having a control gate electrode and a floating gate electrode provided on a semiconductor substrate to have their respective side surfaces in opposed relation, the device comprising:

a gate insulating film formed on the semiconductor substrate;

the control gate electrode formed on the gate insulating film;

a protective insulating film deposited only on that one of the side surfaces of the control gate electrode opposed to the floating gate electrode to protect the control gate electrode during formation of the floating gate electrode;

the floating gate electrode opposed to the side surface of the control gate electrode with the protective insulating film interposed therebetween so as to be capacitively coupled to the control gate electrode;

a tunnel insulating film formed between the floating gate electrode and the semiconductor substrate;

a drain region formed in a region of the semiconductor substrate containing a portion underlying the floating gate electrode; and

a source region formed in a region of the semiconductor substrate opposite to the drain region relative to the control gate electrode.

9. The device of claim 8, wherein the protective insulating film has a uniform thickness.

10. The device of claim 8, wherein the gate insulating film has a uniform thickness.

11. The device of claim 8, wherein the tunnel insulating film has a uniform thickness.

12. The device of claim 8, further comprising an insulating film formed between the control gate electrode and the protective insulating film.

13. The device of claim 8, wherein the protective

insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

14. The device of claim 8, wherein the semiconductor substrate has a stepped portion formed to be covered up with the floating gate electrode.

15. A nonvolatile semiconductor memory device having a control gate electrode and a floating gate electrode provided on a semiconductor substrate to have their respective side surfaces in opposed relation, the device comprising:

a gate insulating film formed on the semiconductor substrate;

the control gate electrode formed on the gate insulating film;

a protective insulating film deposited on that one of the side surfaces of the control gate electrode opposite to the side surface opposed to the floating gate electrode to protect the control gate electrode during formation of the floating gate electrode;

a capacitance insulating film formed on the side surface of the control gate electrode opposed to the floating gate electrode;

the floating gate electrode opposed to the side surface of the control gate electrode with the capacitance insulating film interposed therebetween so as to be capacitively coupled to the control gate electrode;

a tunnel insulating film formed between the floating gate electrode and the semiconductor substrate;

a drain region formed in a region of the semiconductor substrate containing a portion underlying the floating gate electrode; and

a source region formed in a region of the semiconductor substrate opposite to the drain region relative to the control gate electrode.

16. The device of claim 15, wherein the capacitance insulating film has a uniform thickness.

17. The device of claim 15, wherein the protective insulating film has a uniform thickness.

18. The device of claim 15, wherein the gate insulating film has a uniform thickness.

19. The device of claim 15, wherein the tunnel insulating film has a uniform thickness.

20. The device of claim 15, further comprising an insulating film formed between the control gate electrode and the protective insulating film.

21. The device of claim 15, wherein the protective insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

22. The device of claim 15, wherein the semiconductor

substrate has a stepped portion formed to be covered up with the floating gate electrode.

23. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a protective-insulating-film depositing step of selectively removing the second insulating film so as to leave a portion of the second insulating film located on each of side surfaces of the control gate electrode and thereby forming, from the second insulating film, a protective insulating film for protecting the control gate electrode;

a gate-insulating-film forming step of selectively removing the first insulating film so as to leave a portion of the first insulating film underlying the control gate electrode and thereby forming a gate insulating film from the first insulating film;

a tunnel-insulating-film forming step of forming, on the semiconductor substrate, a third insulating film serving as a tunnel insulating film;

a floating-gate-electrode forming step of forming by self alignment a floating gate electrode capacitively coupled to one of side surfaces of the control gate electrode with the protective insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and

a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

24. The method of claim 23, wherein the tunnel-insulating-film forming step includes the step of forming the third insulating film also on the protective insulating film.

25. The method of claim 23, further comprising, between the control-gate-electrode forming step and the second-insulating-film depositing step, the step of:

introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming an insulating film on each of side portions of the control gate electrode.

26. The method of claim 25, wherein the protective-insulating-film forming step includes forming the protective

insulating film by stacking a plurality of insulating films having different compositions.

27. The method of claim 23, wherein the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming the tunnel insulating film, while forming an insulating film having a composition different from a composition of the protective insulating film on a surface of the protective insulating film.

28. The method of claim 23, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

29. The method of claim 23, wherein the semiconductor substrate has a memory circuit formation region including the source region and the drain region and a peripheral circuit formation region to be formed with a peripheral circuit containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

30. The method of claim 29, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

31. The method of claim 29, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.

32. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a sidewall forming step of forming sidewalls over the first insulating film and on portions of the second insulating film located on side surfaces of the control gate electrode;

a protective-insulating-film forming step of performing etching with respect to the first and second insulating films by using the sidewalls and the control gate electrode as a mask and thereby forming, from the second insulating film, a protective insulating film for protecting the control gate electrode on each of the side surfaces of the control gate electrode, while forming, from the first insulating film, a gate insulating film under the control gate electrode;

a tunnel-insulating-film forming step of removing the sidewalls and then forming, in a region in which the semiconductor substrate is exposed, a third insulating film serving as a tunnel insulating film;

a floating-gate-electrode forming step of forming by self alignment a floating gate electrode capacitively coupled to one of the side surfaces of the control gate electrode with the protective insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and

a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

33. The method of claim 32, wherein the tunnel-

insulating-film forming step includes removing the sidewalls and then selectively removing respective portions of the protective insulating film covered with bottom surfaces of the sidewalls.

34. The method of claim 33, wherein the tunnel-insulating-film forming step includes the step of selectively removing the respective portions of the protective insulating film covered with the bottom surfaces of the sidewalls and then selectively removing respective portions of the gate insulating film covered with the bottom surfaces of the sidewalls.

35. The method of claim 32, further comprising, between the protective-insulating-film forming step and the tunnel-insulating-film forming step, the step of:

performing etching with respect to the semiconductor substrate by using the sidewalls as a mask and thereby forming a stepped portion to be covered up with the floating gate electrode in a region of the semiconductor substrate to be formed with the floating gate electrode.

36. The method of claim 32, wherein the tunnel-insulating-film forming step includes the step of forming the third insulating film also on the protective insulating film.

37. The method of claim 32, further comprising, between the control-gate-electrode forming step and the second-insulating-film depositing step, the step of:

introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming an insulating film on each of side portions of the control gate electrode.

38. The method of claim 37, wherein the protective-insulating-film forming step includes forming the protective insulating film by stacking a plurality of insulating films having different compositions.

39. The method of claim 32, wherein the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming the tunnel insulating film, while forming an insulating film having a composition different from a composition of the protective insulating film on a surface of the protective insulating film.

40. The method of claim 32, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

41. The method of claim 32, wherein the semiconductor substrate has a memory circuit formation region including the source region and the drain region and a peripheral circuit

formation region to be formed with a peripheral circuit containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

42. The method of claim 41, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

43. The method of claim 41, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.

44. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a protective-insulating-film forming step of selectively removing the second insulating film so as to leave a portion of the second insulating film located on one of side surfaces of the control gate electrode and thereby forming, from the second insulating film, a protective insulating film for protecting the one of the side surfaces of the control gate electrode;

a gate-insulating-film forming step of selectively removing the first insulating film so as to leave a portion of the first insulating film underlying the control gate electrode and thereby forming a gate insulating film from the first insulating film;

a tunnel-insulating-film forming step of forming, on the semiconductor substrate, a third insulating film serving as a tunnel insulating film;

a floating-gate-electrode forming step of forming by self alignment a floating gate electrode capacitively coupled to the side surface of the control gate electrode with the protective insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

45. The method of claim 44, wherein the tunnel-insulating-film forming step includes the step of forming the third insulating film also on the protective insulating film.

46. The method of claim 44, further comprising, between the control-gate-electrode forming step and the second-insulating-film depositing step, the step of:

introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming an insulating film on each of side portions of the control gate electrode.

47. The method of claim 46, wherein the protective-insulating-film forming step includes forming the protective insulating film by stacking a plurality of insulating films having different compositions.

48. The method of claim 44, wherein the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor

substrate, and thereby forming the tunnel insulating film, while forming an insulating film having a composition different from a composition of the protective insulating film on a surface of the protective insulating film.

49. The method of claim 44, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

50. The method of claim 44, wherein the semiconductor substrate has a memory circuit formation region including the source region and the drain region and a peripheral circuit formation region to be formed with a peripheral circuit containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

51. The method of claim 50, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

52. The method of claim 50, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.

53. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a sidewall forming step of forming sidewalls over the first insulating film and on portions of the second insulating film located on side surfaces of the control gate electrode;

a protective-insulating-film forming step of performing etching with respect to the first and second insulating films by using the sidewalls and the control gate electrode as a mask and thereby forming, from the second insulating film, a protective insulating film for protecting the control gate electrode on each of the side surfaces of the control gate electrode, while forming, from the first insulating film, a gate insulating film under the control gate electrode;

a protective-insulating-film-removing step of removing the sidewalls and then selectively removing the protective insulating film so as to leave a portion of the protective insulating film located on one of the side surfaces of the control gate electrode;

a tunnel-insulating-film forming step of forming, in a region in which the semiconductor substrate is exposed, a third insulating film serving as a tunnel insulating film;

a floating-gate-electrode forming step of forming by self alignment a floating gate electrode capacitively coupled to the side surface of the control gate electrode with the protective insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and

a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

54. The method of claim 53, wherein the protective-insulating-film removing step includes the step of removing the sidewalls and then selectively removing respective portions of the protective insulating film covered with

bottom surfaces of the sidewalls.

55. The method of claim 54, wherein the protective-insulating-film removing step includes the step of selectively removing the respective portions of the protective insulating film covered with the bottom surfaces of the sidewalls and then selectively removing respective portions of the gate insulating film covered with the bottom surfaces of the sidewalls.

56. The method of claim 53, further comprising, between the protective-insulating-film forming step and the protective-insulating-film removing step, the step of:

performing etching with respect to the semiconductor substrate by using the sidewalls as a mask and thereby forming a stepped portion to be covered up with the floating gate electrode in a region of the semiconductor substrate to be formed with the floating gate electrode.

57. The method of claim 53, wherein the tunnel-insulating-film forming step includes the step of forming the third insulating film also on the protective insulating film.

58. The method of claim 53, further comprising, between the control-gate-electrode forming step and the second-insulating-film depositing step, the step of:

introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming an insulating film on each of side portions of the control gate electrode.

59. The method of claim 58, wherein the protective-insulating-film forming step includes forming the protective insulating film by stacking a plurality of insulating films having different compositions.

60. The method of claim 53, wherein the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming the tunnel insulating film, while forming an insulating film having a composition different from a composition of the protective insulating film on a surface of the protective insulating film.

61. The method of claim 53, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

62. The method of claim 53, wherein the semiconductor substrate has a memory circuit formation region including the source region and the drain region and a peripheral circuit formation region to be formed with a peripheral circuit containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the

floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

63. The method of claim 62, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

64. The method of claim 62, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.

65. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a protective-insulating-film forming step of selectively removing the second insulating film so as to leave a portion of the second insulating film located on that one of the side surfaces of the control gate electrode opposite to the side surface to be formed with a floating gate electrode and thereby forming, from the second insulating film, a protective insulating film for protecting the control gate electrode;

a gate-insulating-film forming step of selectively removing the first insulating film so as to remove a portion of the first insulating film underlying the control gate electrode and thereby forming a gate insulating film from the first insulating film;

a capacitance-insulating-film forming step of forming a capacitance insulating film on that one of the side surfaces of the control gate electrode to be formed with the floating gate electrode;

a tunnel-insulating-film forming step of forming a tunnel insulating film on the semiconductor substrate;

a floating-gate-electrode forming step of forming by self alignment the floating gate electrode capacitively coupled to the side surface of the control gate electrode with the capacitance insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and

a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

66. The method of claim 65, wherein the capacitance-insulating-film forming step and the tunnel-insulating-film forming step are composed of identical steps proceeding concurrently.

67. The method of claim 65, wherein the capacitance-insulating-film forming step or the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming the capacitance insulating film or the tunnel insulating film.

68. The method of claim 65, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

69. The method of claim 65, wherein the semiconductor substrate has a memory circuit formation region including the source region and the drain region and a peripheral circuit formation region to be formed with a peripheral circuit

containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

70. The method of claim 69, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

71. The method of claim 69, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.

72. A method for fabricating a nonvolatile semiconductor memory device, the method comprising:

a control-gate-electrode forming step of forming a first insulating film on a semiconductor substrate, patterning a conductor film formed on the first insulating film, and thereby forming a control gate electrode from the conductor film;

a second-insulating-film depositing step of depositing a second insulating film over the entire surface of the semiconductor substrate including the control gate electrode;

a sidewall forming step of forming sidewalls over the first insulating film and on portions of the second insulating film located on side surfaces of the control gate electrode;

a protective-insulating-film forming step of performing etching with respect to the first and second insulating films by using the sidewalls and the control gate electrode as a mask and thereby forming, from the second insulating film, a protective insulating film for protecting the control gate electrode on each of the side surfaces of the control gate electrode, while forming, from the first insulating film, a gate insulating film under the control gate electrode;

a protective-insulating-film removing step of removing the sidewalls and then selectively removing a portion of the protective insulating film located on that one of the side surfaces of the control gate electrode to be formed with a floating gate electrode;

a capacitance-insulating-film forming step of forming a capacitance insulating film on the side surface of the control gate electrode to be formed with the floating gate electrode;

a tunnel-insulating-film forming step of forming a tunnel insulating film in a region in which the semiconductor substrate is exposed;

a floating-gate-electrode forming step of forming by self alignment the floating gate electrode capacitively coupled to the side surface of the control gate electrode with the capacitance insulating film interposed therebetween and opposed to the semiconductor substrate with the tunnel insulating film interposed therebetween; and

a source/drain forming step of implanting an impurity into the semiconductor substrate by using the control gate electrode and the floating gate electrode as a mask and thereby forming a source region and a drain region in the semiconductor substrate.

73. The method of claim 72, wherein the protective-insulating-film removing step includes the step of removing the sidewalls and then selectively removing respective portions of the protective insulating film covered with bottom surfaces of the sidewalls.

74. The method of claim 73, wherein the protective-insulating-film removing step includes the step of selectively removing the respective portions of the protective insulating film covered with the bottom surfaces of the sidewalls and then selectively removing respective portions of the gate insulating film covered with the bottom surfaces of the sidewalls.

75. The method of claim 72, further comprising, between the protective-insulating-film forming step and the protective-insulating-film removing step, the step of:

performing etching with respect to the semiconductor substrate by using the sidewalls as a mask and thereby forming a stepped portion to be covered up with the floating gate electrode in a region of the semiconductor substrate to be formed with the floating gate electrode.

76. The method of claim 72, wherein the capacitance-insulating-film forming step and the tunnel-insulating-film forming step are composed of identical steps proceeding concurrently.

77. The method of claim 72, wherein the capacitance-insulating-film forming step or the tunnel-insulating-film forming step includes the step of introducing hydrogen and oxygen into a space over the heated semiconductor substrate, generating water vapor from the introduced hydrogen and oxygen over the semiconductor substrate, and thereby forming the capacitance insulating film or the tunnel insulating film.

78. The method of claim 72, wherein the second insulating film is a multilayer structure composed of a plurality of stacked insulating films having different compositions.

79. The method of claim 72, wherein the semiconductor substrate has a memory circuit formation region including the

source region and the drain region and a peripheral circuit formation region to be formed with a peripheral circuit containing a field-effect transistor for generating and outputting a drive signal to the control gate electrode, the floating gate electrode, the source region, or the drain region, the method further comprising the step of:

forming the field-effect transistor in the peripheral circuit formation region after forming the source region and the drain region in the memory circuit formation region.

80. The method of claim 79, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of forming also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the formation of the conductor film on the first insulating film.

81. The method of claim 79, wherein the step of forming the control gate electrode in the memory circuit formation region includes the step of patterning also a conductor film for forming a gate electrode of the field-effect transistor simultaneously with the patterning of the conductor film.